Probing the Gate−Voltage-Dependent Surface Potential of Individual InAs Nanowires Using Random Telegraph Signals

Joe Salfi,[†,§,*] Nicola Paradiso,[‡] Stefano Roddaro,[‡] Stefan Heun,[‡] Selvakumar V. Nair,[†,⊥] Igor G. Savelyev,[†,⊥] Marina Blumin,[†,⊥] Fabio Beltram,[‡] and Harry E. Ruda[†,⊥]

[†]Centre for Nanotechnology, University of Toronto, 170 College Street, Toronto, Ontario M5S 3E4, Canada, [‡]NEST, Istituto Nanoscienze-CNR and Scuola Normale Superiore, Piazza S.Silvestro 12, I-56127 Pisa, Italy, [§]Department of Electrical and Computer Engineering, University of Toronto, 10 King's College Road, Toronto, Ontario M5S 3G4, and [⊥]Department of Materials Science and Engineering, University of Toronto, 184 College Street, Toronto, Ontario M5S 3E4

ABSTRACT We report a novel method for probing the gate-voltage dependence of the surface potential of individual semiconductor nanowires. The statistics of electronic occupation of a single defect on the surface of the nanowire, determined from a random telegraph signal, is used as a measure for the local potential. The method is demonstrated for the case of one or two switching defects in indium arsenide (InAs) nanowire field effect transistors at temperatures $T = 25-77$ K. Comparison with a self-consistent model shows that surface potential variation is retarded in the conducting regime due to screening by surface states with density $D_{ss} \approx 10^{12}$ cm^{-2} eV^{-1}. Temperature-dependent dynamics of electron capture and emission producing the random telegraph signals are also analyzed, and multiphonon emission is identified as the process responsible for capture and emission of electrons from the surface traps. Two defects studied in detail had capture activation energies of $E_B \approx 50$ meV and $E_B \approx 110$ meV and cross sections of $\sigma_\infty \approx 3 \times 10^{-19}$ cm^2 and $\sigma_\infty \approx 2 \times 10^{-17}$ cm^2, respectively. A lattice relaxation energy of $S\hbar\omega = 187 \pm 15$ meV was found for the first defect.

KEYWORDS: nanowire · field effect transistors · surface potential · surface states · defects

Owing to their unique geometrical and physical properties and an increasingly sophisticated control over their synthesis,[1,2] semiconductor nanowires grown by the vapor−liquid−solid (VLS) mechanism are of considerable interest for nanoelectronic,[3] photonic,[4] and sensing[5] devices, to name a few. The performance of nanowire-based devices invariably depends on the nanowire's electronic and optical properties, which often differ from those of bulk semiconductors.

In the case of nanowire field effect transistors (FETs) and sensors where surface effects play a critical role, both the carrier mobility and the ability to control the carrier density by an external gate electrode are of primary importance. The latter is a consequence of the relationship between the surface potential of a nanowire and the potential of an external gate electrode, which is determined by density of states in the nanowire combined with geometrical and dielectric parameters of the gate, gate dielectric, and nanowire. Capacitance−voltage ($C-V$) spectroscopy on the gate provides information related to surface potential,[6] but since the gate capacitance $C \approx 100-1000$ aF of nanowires is similar to or below the error of standard capacitance meters, there are only a few studies, and even then, specialized techniques (sub-10 nm gate-dielectric, state-of-the-art instrumentation, and special shielding to eliminate stray capacitance) were used.[7−10] Direct measurements of surface potential of nanowires by Kelvin probe force microscopy[11] (KPFM) have focused on characterization of dopants[12] or built-in potentials at the contact[13] of ungated nanowires. Gate control of the off-state of InAs nanowire field effect transistors was recently considered by Lind and co-workers.[14]

In this paper we report a novel method for extraction of the gate voltage dependence of the surface potential of individual nanowire field effect transistors, based on measurements of the statistical probability of electronic occupation of a single defect site on the nanowire's surface. Stochastic capture and emission of an electron at the defect site is observed in a random telegraph signal (RTS),[15] from which the occupation of the defect is inferred at any given moment. The average occupation probability of the trap observed over many transitions is used to directly obtain the trap energy, and

*Address correspondence to joseph.salfi@utoronto.ca.

Received for review December 9, 2010 and accepted January 25, 2011.

Published online February 15, 2011
10.1021/nn1033967

© 2011 American Chemical Society

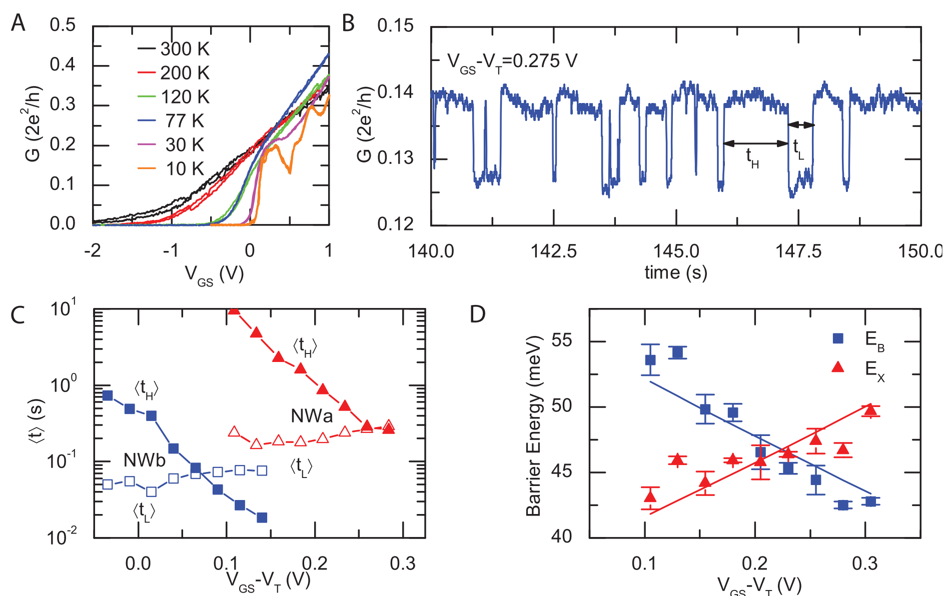

Figure 1. (A) Dependence of conductance on gate voltage for $d = 44 \pm 2$ nm diameter nanowire at several temperatures $T = 10, 30, 77, 120, 200, 300$ K using bias $V = 300\ \mu$V for both increasing and decreasing V_{GS} showing negligible hysteresis. (B) Waveform of stochastic switching of NWa conductance at $T = 40$ K and $V_{GS} - V_T = 0.275$ V, where V_T is the threshold gate voltage to deplete the nanowire when it is in the high conductance state. (C) $\langle t_H \rangle$ (solid points) and $\langle t_L \rangle$ (open points) for NWa (triangles) and NWb (squares). (D) Dependence of activation energies for electron capture (squares, E_B) and emission (triangles, E_X) by defect in NWa for temperatures $34 < T < 43$ K. Lines are least-squares fit of activation energies to multiphonon emission model discussed in the context of Figure 5.

therefore, surface potential energy, relative to the Fermi energy. Put another way, the statistics of time sequences of stochastic fluctuations of charge on a single defect, which is read out by measuring the nanowire's conductance, act as a voltmeter. The results reinforce the notion that the intrinsic signal fluctuations in nanoscale systems are not just "noise". Rather, they may provide important quantitative information about the system's physical properties. In this case, we directly observe the effect of electrostatic coupling that is extremely difficult to measure capacitively in a back-gated nanowire.

We derive the relationship between gate voltage and surface potential in a surround-gate nanowire and, using self-consistent numerical calculations, show how the surface potential develops an appreciable radial asymmetry in back-gated nanowires. The results of these numerical calculations are compared with measured surface potentials for three InAs nanowires in the conducting regime, NWa (59 ± 2 nm diameter) at $T = 40$ K, NWb (28 ± 2 nm diameter) at $T = 25$ K, and NWc (49 ± 2 nm diameter) at $T = 77$ K. NWa and NWb have a single defect capturing and emitting a single electron, and NWc has two simultaneously switching defects. For NWc, calculations reproduce the measured gate-voltage dependence of trap energy when the gate modulates charge in surface states with density $D_{ss} = (1.05 \pm 0.25) \times 10^{12}$ cm^{-2} eV^{-1}, in the linear regime. Similarly, $D_{ss} \approx 10^{12}$ cm^{-2} eV^{-1} is consistent with measured trap energy for both NWa and NWb. The temperature and gate-voltage dependent dynamics for electron capture and emission at the defect are well captured by a theoretical model for multiphonon emission. The lattice distortion energy and cross section[16] associated with capturing an electron on the trap site in NWa are $S\hbar\omega = 187 \pm 15$ meV and $\sigma_\infty \approx 3 \times 10^{-19}$ cm^2, respectively. Another defect studied in NWa has $\sigma_\infty \approx 2 \times 10^{-17}$ cm^2. The small capture cross sections support the notion that RTS occurs due to capture and emission of carriers from traps probably residing at the border or just inside the 2−3 nm native oxide of the nanowire.

InAs nanowires were grown by molecular beam epitaxy (MBE) and transferred to a degenerately doped silicon substrate coated with 100 nm of SiO_2. Two Ni/Au ohmic contacts separated by a distance of 600 nm (NWa) or 1 μm (NWb, NWc) were deposited on individual InAs nanowires, and used to measure their two terminal conductance, which decreases with decreasing (back-gate) voltage V_{GS}. The conductance was measured using a bias $V < k_B T$, where T is the temperature and k_B is the Boltzmann constant, to avoid any possibility of heating the carrier gas. The dependence of conductance on gate voltage for a typical InAs nanowire is shown in Figure 1A for temperatures between $T = 10$ and $T = 300$ K. The electron density and field effect mobility of our InAs nanowires, extracted as described in the Methods section, are nominally $n_o \approx 10^{17}$−10^{18} cm^{-3} and $\mu_{FE} \approx 2000$−4000 cm^2 V^{-1} s^{-1} at room temperature, respectively. The latter is typically 10000−20000 cm^2 V^{-1} s^{-1} at 30 K.

RESULTS AND DISCUSSION

Approximately one-third of devices fabricated exhibit random telegraph signals such as the one shown in Figure 1B for NWa at 40 K. The distribution of times t_H (t_L) spent in the state with high (low) conductance obey Poisson statistics, characterized by a mean time $\langle t_H \rangle$ ($\langle t_L \rangle$). Shown in Figure 1C, $\langle t_H \rangle$ decreases with increasing gate voltage and $\langle t_L \rangle$ slightly increases, so that overall, the relative probability $\langle t_H \rangle / \langle t_L \rangle$ decreases. Since the difference between the trap energy and Fermi energy decreases with increasing gate voltage, increasing the probability of trap occupancy, we conclude that the low conductance state corresponds to the situation when the defect has captured an electron. Characteristic times $\langle t_H \rangle$ and $\langle t_L \rangle$ exhibit thermally activated behavior with $\langle t_H \rangle^{-1} = nC_n \exp(-\beta E_B)$ and $\langle t_L \rangle^{-1} = nE_n \exp(-\beta E_X)$. Here, E_B and E_X are the activation energies for electron capture and emission, respectively, C_n and E_n are electron capture and emission coefficients, respectively, n is the electron density which is essentially temperature independent, and $\beta = 1/k_BT$. The electronic $1/f$ noise, studied in VLS-grown InAs nanowires by Sakr and Gao,[17] is normally ascribed to ensembles of related electron trapping centers having a dispersion of activation energies.[15] The gate voltage dependence of the $\approx$50 meV capture and emission activation energies for the defect responsible for the random telegraph signal in NWa are shown in Figure 1D. We infer that the microscopic process responsible for capture and emission is a thermally activated multiphonon emission process relevant for deep levels in semiconductors,[16] and later identified as the mechanism responsible for random telegraph noise in silicon inversion layer structures.[15,18,19] In the multiphonon emission model, the barriers E_B and E_X are signatures of lattice perturbation associated with the localized nature of the captured electron. Cascade-capture and Auger-assisted trapping can be ruled out, since the rates for such processes have a weak power-law temperature dependence.[20]

The relative probability of the defect being unoccupied, $\langle t_H \rangle / \langle t_L \rangle$, can be known to nearly 1% precision from an RTS with a few thousand transitions, and can be understood quantitatively by considering the trap subsystem, which is capable of exchanging electrons with the nanowire, in the context of the grand canonical ensemble.[21] We obtain $\ln(\langle t_H \rangle / \langle t_L \rangle) + \ln(g) = \beta(E_T - E_F)$ where $E_T = E(N) - E(N-1)$ and $g = \gamma(N)/\gamma(N-1)$ are the trap level energy and degeneracy, respectively, and $E(n)$ and $\gamma(n)$ are the energy and degeneracy of the n electron state of the defect.[22] Here, β corresponds to the common temperature of the nanowire and defect subsystem, and E_F is their common Fermi energy.[22] The trap energy E_T includes the gate voltage dependent interaction between trapped charge and electrons in the nanowire's conduction band, in addition a gate voltage independent term E_T^0. The latter is

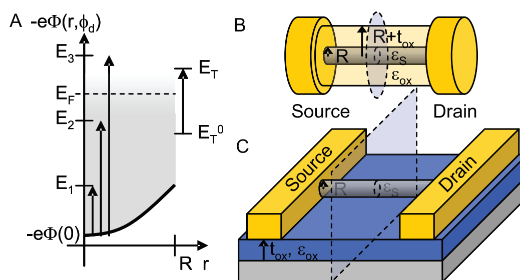

Figure 2. (A) Radial variation of electrostatic potential energy in nanowire of radius R depleted of electrons by a negative gate voltage V_{GS} at a particular angle ϕ_d. Electron sub-band edges E_1, E_2, and E_3, and trap level $E_T = E_T^0 - e\Phi(R,\phi_d)$ are superimposed. (B) Coaxial gate at radial coordinate $R + t_{ox}$ surrounding nanowire with radius R by dielectric ε_{ox}, and plane of cross-section (dashed). (C) Planar back-gate geometry separated from nanowire by a film of SiO_2 of thickness t_{ox} = 100 nm, and plane of cross-section (dashed).

the sum of the ionic interaction energy of the lattice distortion created when the localized trap level is filled, and the electronic level produced by the deep electron-ion potential of the trap.[18,19] Owing to the Pauli principle and finite density of states in the nanowire, increasing the gate voltage (and therefore, electron density) decreases the electronic energy of a trap relative to the Fermi energy.

The relationship between the energy of the localized trap state and surface potential is given by $E_T = E_T^0 - e\Phi(\vec{r}_d)$, where $\Phi(\vec{r})$ is the electrostatic potential, and $\vec{r}_d = \hat{r}(\phi)R$ is the position of the defect on the nanowire's surface. The free electron density in the nanowire is given by

$$n(\vec{r}) = \sum_i n'_i(E_F + e\Phi(0) - E_i, T)|\varphi_i(r, \phi)|^2 \quad (1)$$

where $n'_i(E_F + e\Phi(0) - E_i, T)$ is the linear electron density for the ith sub-band with edge energy E_i above the electrostatic potential energy $-e\Phi(0)$ at the center of the nanowire, and $\varphi_i(r,\phi)$ is the electron wave function for the ith sub-band in the $X-Y$ plane perpendicular to the nanowire's axis. Quantities $\varphi_i(r,\phi)$ and E_i must be determined self-consistently with the electrostatic potential $\Phi(\vec{r})$, which is governed by the Poisson equation

$$\nabla \cdot (-\varepsilon(\vec{r})\nabla\Phi(\vec{r})) = \rho(\vec{r}) = e(N_D - n(\vec{r})) + \rho_s \quad (2)$$

where $\varepsilon(\vec{r})$ is the position-dependent dielectric permittivity of the system and $\rho(\vec{r})$ is a charge density comprising uniform background density eN_D of ionized donors, the free electron charge density $-en(\vec{r})$, and a surface charge density ρ_s at radial coordinate $r = R$. The electrostatic potential energy, trap energy, and sub-band minima are illustrated schematically in Figure 2A.

An illustrative special case of the above is that of a coaxial-gate with radius $R + t_{ox}$ separated from a nanowire with radius R by a dielectric with permittivity ε_{ox}. For the moment we take $\rho_s = 0$. The radially symmetric electrostatic potential in a cross section of the coaxial gate structure shown in Figure 2B is obtained by integrating

the Poisson equation. The result at $r = R$ is

$$\Phi(R) - \Phi(0) = -\frac{eR^2 N_D}{4\varepsilon_s} + \frac{e}{\varepsilon_s}\sum_i F_i n'_i(E_F + e\Phi(0) - E_i, T) \quad (3)$$

where $F_i = \int_0^R dr_2/r_2 \int_0^{r_2} dr_1 r_1 |\varphi_i(r_1)|^2$ is a dimensionless constant, and ε_s is the dielectric constant for the semiconductor nanowire. Substituting $E_T = E_T^0 - e\Phi(R)$, we obtain the variation of trap energy with respect to the Fermi energy, parametrized in terms of $E_F + e\Phi(0)$

$$E_T - E_F = E_T^0 + \frac{e^2 R^2 N_D}{4\varepsilon_S} - \frac{e^2}{\varepsilon_S}\sum_i F_i n'_i(E_F + e\Phi(0) - E_i, T) - (E_F + e\Phi(0)) \quad (4)$$

In experiments, V_{GS} controls the surface potential $\Phi(R)$, and the relationship between V_{GS} and $E_F + e\Phi(0)$ is obtained by integration of the Poisson equation to the gate boundary, giving $\Phi(R + t_{ox}) = \Phi(R) + R\, d\Phi/dr|_{r\to R^+} \ln((R + t_{ox})/R)$. Employing boundary conditions $d\Phi/dr|_{r\to R+} = \varepsilon_s/\varepsilon_{ox}\ d\Phi/dr|_{r\to R-} = -e/(2\pi\varepsilon_{ox}R) \sum_i n'_i(E_F + e\Phi(0) - E_i, T)$ and $-e\Phi(R + t_{ox}) = E_F - eV_{GS}$ we obtain V_{GS} parametrized in terms of $E_F + e\Phi(0)$:

$$V_{GS} = -\frac{E_T - E_F}{e} + \frac{en'}{C'_G} \quad (5)$$

where $n' = \sum_i n'_i(E_F + e\Phi(0) - E_i, T)$ and $C'_G = 2\pi\varepsilon_{ox}/\ln((R + t_{ox})/R)$ are the electron density and geometrical gate capacitance per unit length, respectively. We define $\alpha(V_{GS}) = \partial(E_T - E_F)/\partial V_{GS}$, and using eq 5 we obtain $\alpha(V_{GS}) = e(C'/C'_G - 1)$, where $C' = e\partial n'/\partial V_{GS}$ is the total gate capacitance. In the single subband case, $C' \approx (F_1/\varepsilon_s + C'^{-1}_G + C'^{-1}_Q)^{-1}$, where $C'_Q = e^2\partial n'/\partial E_F$ is the quantum capacitance.[23] The main insight provided by these analytical results is that, provided the geometrical capacitance C'_G is not by far the largest contribution to the total capacitance C', $\alpha(V_{GS})$ contains an appreciable contribution from density of states (C_Q) and electrostatics (F_1). Moreover, these contributions can be easily and directly evaluated from expressions 4 and 5, given an appropriate density of states.

The planar back-gate shown in the schematic Figure 2C breaks the radial symmetry of potential in the nanowire FET, which has to be taken into account for quantitative comparison of the dependence of $E_T - E_F$ on gate voltage V_{GS}, between theory and experiments. Below we compare self-consistent numerical calculations of the dependence of trap energy on gate voltage to the experimentally extracted trap energies $E_T - E_F = k_B T \ln(\langle t_H\rangle/\langle t_L\rangle)$, for NWa, NWb, and NWc, ignoring the small, gate voltage independent contribution $k_B T \ln(g)$. The measured nanowire radii R and gate dielectric thickness t_{ox} are taken into account in eq 2, along with realistic dielectric constants for InAs ($\varepsilon_s = 15.5\varepsilon_0$) and SiO_2 ($\varepsilon_{ox} = 3.9\varepsilon_0$), where ε_0 is the vacuum permittivity. For eq 1, the sub-band energies corresponding to an infinite cylindrical well, $E^0_{m,l} = \hbar^2\xi^2_{m,l}/(2m_e R^2)$, are corrected to leading order in Φ, giving

$$E_{m,l} = E^0_{m,l} + \langle m, l| - e\Phi(r, \phi)|m, l\rangle \quad (6)$$

with envelope wave functions[24] $\varphi_{m,l}(r,\phi)$ proportional to the cylindrical Bessel functions $J_{|l|}(\xi)$; *i.e.*,

$$\varphi_{m,l}(r, \phi) = J_{|l|}(\xi_{m,l} r/R)\exp(-il\phi)/(\sqrt{\pi}RJ_{|l|+1}(\xi_{m,l})) \quad (7)$$

where $l = 0, \pm1, \pm2, ...,$ and $\xi_{m,l}$ is the mth root of $J_{|l|}(\xi)$. The effective mass m_e of electrons is taken from bulk band structure of zincblende InAs. The one-dimensional electron density $n'_{m,l}$ for the sub-band with indices m and l is obtained by integrating over phase space,

$$n'_{m,l} = 2(2\pi m_e k_B T/h^2)^{1/2}\mathscr{F}_{-1/2}(\eta_{m,l}) \quad (8)$$

where $\eta_{m,l} = \beta(E_F - E_{m,l})$, $\mathscr{F}_j(\eta) = 1/\Gamma(j+1)\int_0^\infty du\,u^j - (1+\exp(u-\eta))^{-1}$ is the complete Fermi-Dirac integral of order j, and $\Gamma(x)$ is the gamma function. This approach is justified since only one or two sub-bands should be occupied, in our experiments, as we will see from results of the calculations. Gate-induced modulation of charge in surface states is included using a simple model employing a spatially continuous surface state density with a uniform energy distribution. The surface charge density is expressed as $\rho_s = ek_B T D_{ss}\,\mathscr{F}_{0d}(\eta_s)$ where D_{ss} is the density of surface states, $\mathscr{F}_{0d}(\eta_s) = \int_0^\infty du(1+2\exp(u-\eta_s))^{-1}$ describes donor occupation, $\eta_s = \beta(E_{CNL} - e\Phi(R,\phi) - E_F)$, and E_{CNL} is a surface charge neutrality level.[25,26]

The theoretically calculated variation of trap energy with gate voltage is plotted along selected angles ϕ for NWa and NWb in Figure 3 panels A and B, respectively, together with experimentally extracted trap energy. First, we note that the planar back-gate has induced radial assymmetry in the calculated surface potential in the nanowire. As expected, trap energies toward the bottom of the nanowire ($\phi = -\pi/2$) vary more rapidly with gate voltage than those on the top ($\phi = \pi/2$). For NWa with diameter $d = 59$ nm, the measured trap energy fits well the calculated surface potential with $D_{ss} = 0$. For NWb with diameter $d = 28$ nm, a surface state density of at least $D_{ss} = 8 \times 10^{11}$ cm^{-2} eV^{-1} is required to obtain a reasonable fit with experiments. Otherwise $|\alpha(V_{GS})|$ is too large. We remark that D_{ss} is the only tunable parameter in our calculation. The charge neutrality level E_{CNL}, background ionized donor concentration N_D, and fixed charge determine only the predicted threshold voltage V_T of cylindrical nanowires in our model,[27] and have no other effect on $\alpha(V_{GS})$. Comparing Figure 3 panels A and B, we also see that $\alpha(V_{GS})$ varies more with respect to ϕ for larger diameter nanowires, as expected. Plotted on the right y-axis in Figure 3 panels A and B are the calculated quantities $\partial n'/\partial E_F$ for NWa and NWb. The Van Hove singularities

due to the quasi-one-dimensional density of states are significantly thermally broadened. Nevertheless, we can identify that the electron density is sufficient to partially fill the second sub-band at $V_{GS} - V_T \approx 0.1$ V in NWa, but not for NWb, a consequence of the larger sub-band splitting for the smaller diameter nanowire.

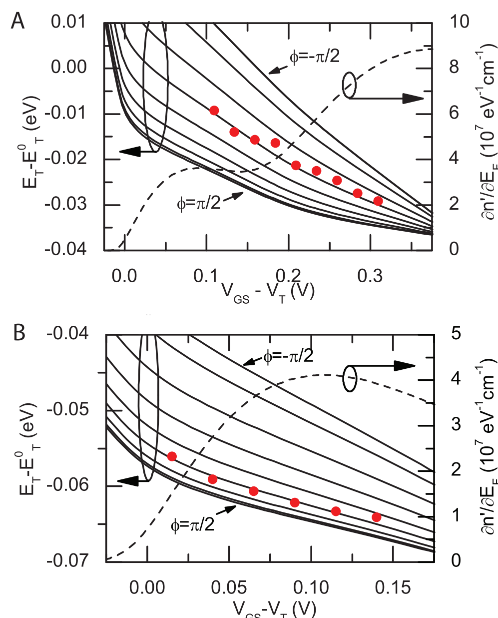

Figure 3. Gate-voltage dependence of measured trap energy $E_T - E_T^0 = -e\Phi(R)$ (red circles), and calculated trap energy using the model described in the main text, for angles $\phi = \pm\pi/2, \pm3\pi/8, \pm\pi/4, 0$, and density of states $\partial n'/\partial E_F$ for (A) NWa with $d = 59$ nm at $T = 40$ K and (B) NWb with $d = 28$ nm at $T = 25$ K.

Another interesting case is that of two traps A and B that are both capturing and emitting electrons in the same nanowire. This process produces a RTS with four distinct levels, as shown in Figure 4A for NWc. We denote t_{ij} as an interval of time with trap A and B in states $i \in \{0,1\}$ and $j \in \{0,1\}$, respectively, where 0 means the trap is empty, 1 means it is full. If the traps are located sufficiently close together compared to the electronic screening length then an electron captured in trap A will change the energy level of trap B and vice versa, and the statistics for the traps will be correlated.[28] The trapping energy of defect A can be evaluated from experimental data for the case when defect B is empty, $E_{TA}|_{B0} - E_F = k_B T \ln(\Sigma_k t_{10}^k / \Sigma_k t_{00}^k)$ or when it is filled $E_{TA}|_{B1} - E_F = k_B T \ln(\Sigma_k t_{11}^k / \Sigma_k t_{01}^k)$. Here, $\sum_k t_{ij}^k$ is the sum of individual intervals of time t_{ij}^k spent in the state ij.

Trap energies are shown in Figure 4B for both trap A (red squares) and B (blue circles) when the other trap is filled (solid points) or empty (open points). The symbol size is approximately equal to the measurement uncertainty which stems from the finite number of defect transitions observed per gate voltage. The energy differences $E_{TA}|_{B1} - E_{TA}|_{B0}$ and $E_{TB}|_{A1} - E_{TB}|_{A0}$ are of the same order as the measurement uncertainty, which is a few meV. In other words, the energy of trap A is not dependent on whether or not trap B is filled with an electron, and vice versa, to within experimental error. For the two traps to not interact in this manner, they must be physically located at positions in the nanowire which are several screening lengths apart. Second, the energy of trap A has a stronger dependence on gate voltage compared with the energy of trap B. The

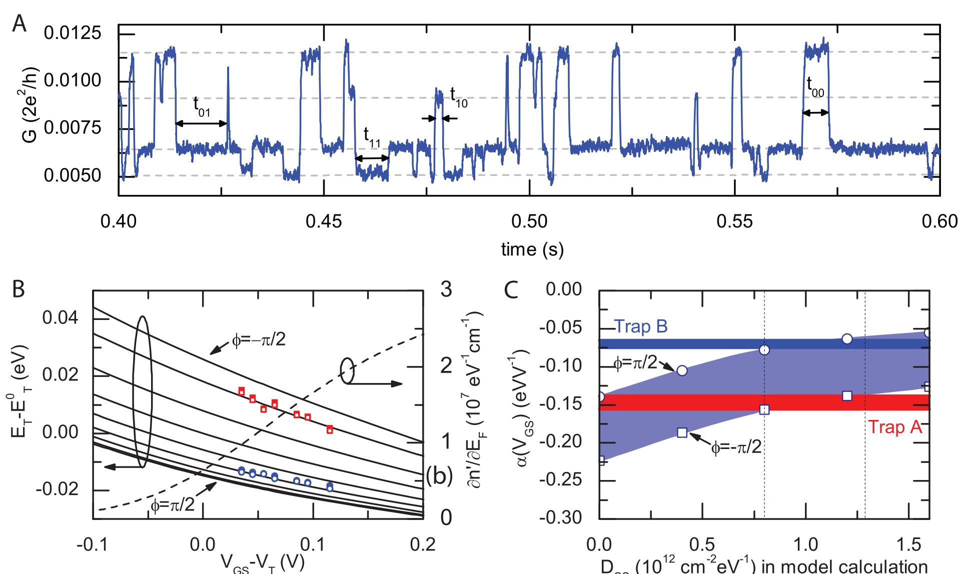

Figure 4. (A) Random telegraph signal for NWc with four levels of conductance due to capture and emission of electrons from two different defects A and B. (B) Measured trap energy at defect A (red squares) and defect B (blue circles), inferred from times t_{ij}, when either trap is either empty (open points) or filled (solid points), and calculated trap energy using model described in the main text, and density of states $\partial n'/\partial E_F$ for the same gate voltages. (C) Plot showing surface state density range $D_{ss} = (1.05 \pm 0.25) \times 10^{12}$ cm^{-2} eV^{-1} where $\alpha(V_{GS})$ extracted by a linear fit of the measured data for trap A (red) and trap B (blue) matches the shaded region (light blue) bounded by splines passing through values of α calculated for $D_{ss} = 0, 0.4, 0.8, 1.2$, and 1.6×10^{12} cm^{-2} eV^{-1} (open symbols).

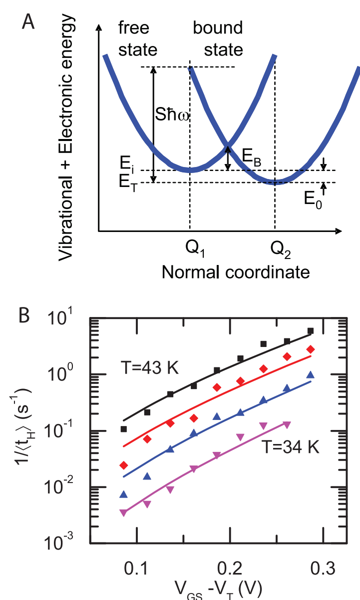

Figure 5. (A) Configuration coordinate diagram demonstrating electronic + vibrational energy of free and bound electronic states with thermal equilibrium normal coordinates of Q_1 and Q_2, respectively. Barrier energy E_B and lattice relaxation energy $S\hbar\omega$ are indicated. (B) Capture rate $\langle t_H \rangle^{-1}$ for NWa at different gate voltages and temperatures T = 43(black squares), 40 (red diamonds), 37 (blue triangles), and 34 K (inverted magenta triangles), and least-squares fit to expression described in main text.

calculated trap energies for different angles ϕ are plotted alongside data points in Figure 4B for D_{ss} = 1.6×10^{12} cm^{-2} eV^{-1}. Calculated values of $\alpha(V_{GS})$ match those inferred from measured trap energies for $D_{ss} = (1.05 \pm 0.25) \times 10^{12}$ cm^{-2} eV^{-1} for NWc at 77 K, as shown in Figure 4C. From these results we can estimate that a gate voltage δV_{GS} = 100 mV beyond V_T fills $\alpha(V_{GS})\delta V_{GS} 2\pi R D_{ss} \approx 15$ electrons/μm in surface states and $\int_{VT}^{VT+\delta V_{GS}} dV_{GS}\, \partial n'/\partial E_F \alpha(V_{GS}) \approx 15$ electrons/μm in the conduction band.

Finally, we elaborate on the microscopic process producing electron trapping and emission dynamics, providing further support for our trap energy model. We focus on NWa, for which we captured a series of RTS at different gate voltages and temperatures, since it exhibits typical behavior. The capture and emission rates $\langle t_H \rangle^{-1}$ and $\langle t_L \rangle^{-1}$ are both thermally activated, with measured activation energies summarized in Figure 1D. The net result of the capture (emission) process, shown schematically in the configuration coordinate diagram in Figure 5A, is a free-to-bound (bound-to-free) electronic transition, coupled with build-up (release) of a lattice distortion induced by the electron−phonon interaction between the localized electronic state, and the lattice. The capture (emission) process occurs when there is sufficient thermally induced distortion of the lattice about normal coordinate Q_1 (Q_2) that the electron−phonon interaction can mediate a transition between the free and bound electronic states. Immediately after the transition the lattice is significantly out of equilibrium, and several phonons are emitted so that the lattice relaxes to the normal coordinate Q_2 (Q_1). Theories for multiphonon emission associate the capture and emission activation energies E_B and E_X with the lattice distortion required to produce a crossing between the two states.[16,29] The capture energy barrier E_B can be rewritten as $E_B = (E_0 - S\hbar\omega)^2/4S\hbar\omega$, where S is the Huang−Rhys factor, the number of phonons of energy $\hbar\omega$ making up the lattice distortion energy $S\hbar\omega$, as shown on the configuration coordinate diagram (Figure 5A). Electrons are assumed to be captured from the Fermi energy E_F of the nanowire, such that $E_0 = E_F - E_T$. Ignoring the possibility that different electronic subbands may have different capture constants, we write the overall capture rate as

$$\langle t_H \rangle^{-1} = nC_{n0} \exp\left(-\beta \frac{(E_F - E_T - S\hbar\omega)^2}{4S\hbar\omega}\right) \quad (9)$$

where n is the electron density in the nanowire. The measured capture rate is shown in Figure 5B for four temperatures T = 43, 40, 37, and 34 K. Using our electrostatic model for n and experimentally measured variation of $E_T - E_F$, we performed least-squares fits of the capture rate data to the expression, obtaining a capture coefficient $C_{n0} = (1.5 \pm 0.5) \times 10^{-11}$ cm^{-3}/s and $S\hbar\omega = 187 \pm 15$ meV corresponding to approximately eight optical phonons in bulk InAs. The best-fit two-parameter model reproduces very well both the measured gate-voltage dependence of capture rate (Figure 5B) and activation energy (Figure 1D).

The capture coefficient is often represented as $C_{n0} = v\sigma_\infty$ where v is the average carrier velocity and σ_∞ is the capture cross section. Experimentally we find that carrier concentration is essentially temperature independent in the regime of Figure 5B, and the calculated Fermi velocity $v_F = \hbar/m_e(3\pi^2 n)^{1/3} \approx 5 \times 10^7$ cm/s exceeds the thermal velocity $v_{th} = (3k_BT/2)^{1/2} \approx 2 \times 10^7$ cm/s of carriers, so $v = v_F$ is used, giving $\sigma_\infty \approx 3 \times 10^{-19}$cm^2. Capture and emission rates were measured using the same procedure for a different trap in the same wire but at a temperature of 58−75 K. This defect also fits very well the thermally activated behavior with $E_B = 114 \pm 2$ meV and $\sigma_\infty \approx (2.2 \pm 1.1) \times 10^{-17}$ cm^2, as shown in the Supporting Information. Cross sections 10^{-19}−10^{-17} cm^2 are a bit low for electronic deep levels in semiconductors, but not for bound electronic states at the border of or just inside the 2−3 nm thick native oxide of the InAs nanowire. In this case, the modulus squared of the transition matrix element between the free and bound state, encapsulated by C_{n0} in the theory, is dramatically suppressed.[18,19]

The condition $t_H/t_L = 1$, or equivalently $E_T \approx E_F$, is normally found for $V_{GS} > V_T$ in our InAs nanowires that exhibit RTS. The latter corresponds to $E_F \gtrsim E_{1,0}$ at low temperatures, so the trap energies satisfy $E_T \gtrsim E_{1,0}$, that is, they are nearly resonant with or just above the conduction band edge of the InAs nanowire. On the basis of the values of the electron capture cross sections measured, it is reasonable to assume that the

traps are located inside the disordered native oxides[30] InO_x and AsO_x or at their interface with the InAs nanowire. Controlled electronic passivation of the InAs surface to reduce surface state density and improve electronic mobility is a topic of much current interest.[31−33] Further improvement of electronic properties are likely as growth and passivation methodology for bare InAs and InAs core/shell nanowires improves. The measured field effect mobility of our bare InAs nanowires is comparable to the highest reported values for InAs.[8,31,33]

Some general remarks about the measurement method for surface potential are in order. The defect level, whose trapping/detrapping statistics we use to extract surface potential, produces a change in current of 1−10 nA in our 30−60 nm diameter InAs NWs at 1 mV bias. This is a consequence of the high sensitivity of conductance of nanowires to localized repulsive charges.[34] In comparison, the gate capacitance $C \approx 100$ aF of a long-channel back-gated nanowire is similar to the error of standard capacitance meters. After all, $C = 100$ aF produces only $dI = 2\pi fC\,dV \approx 12$ fA of displacement current using a modulation voltage $dV = 10$ mV alternating at $f = 1$ kHz, and only $dI = 2\pi fe = 1$ fA displacement current per electron. Moreover, as length of the gate shrinks, C is further reduced making capacitance measurements more difficult, but the changes in conductance due to trapping and emission do not become more difficult to measure.

Additionally, the measured quantity $E_T - E_F$, which can be expressed as $e(C/C_G - 1)\,dV_{GS}$ in the coaxial gate case, always increases with increasing surface state density, "stretching out" its dependence on V_{GS} in just the same way that the $C-V$ curve is stretched out due to interface states.[6] We estimate $D_{ss} \approx 10^{12}$ cm^{-2} eV^{-1} in the temperature range 25−77 K. This value is higher than those obtained from temperature-dependent $C-V$ measurement of InAs nanowires by Ford and co-workers,[8] who also found a freezeout of surface-state modulation at 77 K in their $f = 1$ and 10 kHz capacitance measurements. It is likely that our trap energies include effects of charge redistribution in surface states that are frozen out in their experiments performed at $f = 1$ kHz, though differences in sample preparation/measurement cannot be ruled out. Indeed, the method reported herein lends itself naturally to the study of slow processes, since arbitrarily long random telegraph signals can be captured, and the capture can take place an arbitrary time after each change of gate voltage. Most importantly these slow processes must play a role in $I-V_{GS}$ measurements on nanowires commonly used to estimate field effect mobility, when the sweep time for the gate voltage is comparable to the emission/trapping rate, which could easily be slower than the $C-V$ measurement frequency. Therefore, the method described is not only advantageous for measuring gate coupling when there are only a few charges being modulated, but can potentially provide information about slow surface states that may be even more difficult to obtain by $C-V$ measurements. Our InAs nanowires typically have a subthreshold slope of $S = 170$ mV (per decade) at $T = 77$ K. The equivalent surface state capacitance C_{ss} can be readily obtained from the subthreshold slope[6,27] using $S = \ln(10)(k_BT/e)(C_G + C_{ss})/C_G$, giving a surface state density $D_{ss} = e^{-2}C_{ss}/(2\pi RL) \approx 2 \times 10^{12}$ cm^{-2} eV^{-1} similar to the value estimated from the surface potential−gate voltage relationship. Lind and co-workers[14] found that a similar surface charge density was consistent with measured subthreshold characteristics of InAs nanowire transistors. Similar, gate-dependent measurements of capture rate or surface potential performed at lower temperatures than those used in our experiments may present some evidence of the characteristic Van Hove singularities, as they pass through the Fermi energy. When the gate oxide is very thin (<10 nm), a contribution to the trap energy from polarization induced on the gate may need to be taken into account.[19,35]

In conclusion, the gate-voltage dependence of surface potential of InAs nanowires was investigated by a novel method, using the statistics of electronic occupation of one or two surface traps, inferred from a random telegraph signal. The method provides direct insight into surface potential modulation in nanowires, of much relevance for nanoelectronic and sensing applications. Measured quantities were reconciled with a theoretical model, requiring surface state density $D_{ss} \approx 10^{12}$ cm^{-2} eV^{-1} for quantitative agreement. The temperature dependence of the electron capture and emission dynamics was used to determine the lattice relaxation energy $S\hbar\omega = 187 \pm 15$ meV for one defect and an approximate capture cross sections of $\sigma_\infty \approx 3 \times 10^{-19}$ cm^2 and $\sigma_\infty \approx 2 \times 10^{-17}$ cm^2 for two defects responsible for RTS.

METHODS

Nanowire Growth. InAs nanowires were grown by solid-source molecular beam epitaxy[36] on the (100) surface of GaAs seeded by gold droplets formed by *in situ* gold deposition and annealing. No intentional doping was carried out.

Nanowire Device Fabrication. Electrodes were patterned spaced $L = 1000$ nm (NWb, NWc) or 600 nm apart (NWa) on InAs nanowires deposited on p++ Si wafers coated with 100 nm of SiO_2 fabricated by a standard dry thermal oxidation process. After electron beam lithography to open contact windows, samples were exposed to remote oxygen plasma for 8 s at a

oxygen pressure of 10^{-1} mbar and dipped in ammonium polysulfide (0.3% by weight in deionized water) for several minutes to passivate their surfaces. Immediately after the passivation, they were loaded into an evaporator chamber that was pumped for 30 min down to a pressure of $2-3 \times 10^{-7}$ mbar, followed by deposition of Ni/Au (10 nm/100 nm) (NWa, NWB) or Ti/Au (10 nm/100 nm) (NWc) bilayer ohmic contacts.

Measurements. The Si/SiO_2 substrates with electrically contacted nanowires were cleaved and wirebonded into commercial ceramic chip carriers. During electrical measurements, the chip carrier was held in a vacuum better than 10^{-4} mbar, either in a closed cycle He cryostat (NWa, NWb) or thermally anchored in the inner vacuum chamber of a He cryostat that was cooled with LN2. Current measurements were made using a variable-gain, low-noise current preamplifier, and random telegraph signals recorded by a digital sampling oscilloscope (NWa, NWb) or a fast, buffered digital voltmeter (NWc). Field effect mobility and carrier density are extracted using the standard method employing the charge control model $n_0 = CV_T/(e\pi R^2 L)$ and $\mu_{FE} = \partial I/\partial V_{GS} L^2/(CV)$ taking the gate capacitance C as equal to the geometrical capacitance $C = 2\pi\varepsilon_{eff}/\text{arccosh}((t_{ox} + R)/R)$. Here, V_T is the threshold voltage, V_{GS} is the applied gate voltage, V is the applied source-drain bias, I is the measured current, and R is the measured nanowire radius, L is the measured distance between source and drain contacts, t_{ox} is the measured dielectric thickness, and ε_{eff} is an effective dielectric constant.[37]

Statistics. Random telegraph signals with several thousand transitions were converted into sequences of times t_H and t_L using both threshold values and edge detection algorithms,[38] and later with hidden Markov model parameter estimators.[39] Owing to the large signal-to-noise ratio inherent to our measurements, all three methods produced indistinguishable results.

Acknowledgment. The authors would like to thank D. G. Austing for helpful discussions, M. G. House for pointing out his paper on hidden Markov models (HMMs)[39] which was useful in our analysis, and Y. Ma for reviewing the manuscript. Authors J.S., S.V.N., I.G.S., M.B., and H.E.R. gratefully acknowledge financial support from the Natural Sciences and Engineering Research Council of Canada, the Canadian Space Agency, the Canadian Institute for Photonic Innovations, the Ontario Challenge Fund, and the Ontario Centres of Excellence Program. Authors N.P., S.R., S.H. and F.B. acknowledge the FIRB project RBIN067A39 "Semiconduttori unidimensionali autoassemblati e loro applicazioni dispositivistiche".

Supporting Information Available: Additional capture rate data for NWa. This material is available free of charge *via* the Internet at http://pubs.acs.org.

Note Added after ASAP Publication. After this paper was published online February 15, 2011, corrections were made to the text and to Figures 3 and 4. The revised version was published February 22, 2011.

REFERENCES AND NOTES

1. Fan, H. J.; Werner, P.; Zacharias, M. Semiconductor Nanowires: From Self-Organization to Patterned Growth. *Small* **2006,** *2*, 700–717.
2. Dick, K. A.; Caroff, P.; Bolinsson, J.; Messing, M. E.; J., J.; Deppert, K.; Wallenberg, L. R.; Samuelson, L. Control of III−V Nanowire Crystal Structure by Growth Parameter Tuning. *Semicond. Sci. Technol.* **2010,** *25*, 024009.
3. Lu, W.; Xie, P.; Lieber, C. M. Nanowire Transistor Performance Limits and Applications. *IEEE Trans. Elec. Dev.* **2008,** *55*, 2859–2876.
4. Yan, R.; Gargas, D.; Yang, P. Nanowire Photonics. *Nat. Photonics.* **2009,** *3*, 569–576.
5. Ramgir, N. S.; Yang, Y.; Zacharias, M. Nanowire-Based Sensors. *Small* **2010,** *6*, 1705–1722.
6. Sze, S. M. *Physics of Semiconductor Devices*; John Wiley: NJ, 2007; pp 198, 219, 314−315.
7. Tu, R.; Zhang, L.; Nishi, Y.; Dai, H. J. Measuring the Capacitance of Individual Semiconductor Nanowires For Carrier Mobility Assessment. *Nano Lett.* **2007,** *7*, 1561–1565.
8. Ford, A. C.; Ho, J. C.; Chueh, Y. L.; Tseng, Y. C.; Fan, Z. Y.; Guo, J.; Bokor, J.; Javey, A. Diameter-Dependent Electron Mobility of InAs Nanowires. *Nano Lett.* **2009,** *9*, 360–365.
9. Garnett, E. C.; Tseng, Y. C.; Khanal, D. R.; Wu, J. Q.; Bokor, J.; Yang, P. D. Dopant Profiling and Surface Analysis of Silicon Nanowires Using Capacitance−Voltage Measurements. *Nat. Nanotechnol.* **2009,** *4*, 311–314.
10. Roddaro, S.; Nilsson, K.; Astromskas, G.; Samuelson, L.; Wernersson, L. E.; Karlstrom, O.; Wacker, A. InAs Nanowire Metal−Oxide−Semiconductor Capacitors. *Appl. Phys. Lett.* **2008,** *92*, 253509.
11. Nonnenmacher, N.; O'Boyle, M. P.; Wickramasinghe, H. K. Kelvin Probe Force Microscopy. *Appl. Phys. Lett.* **1991,** *58*, 2921–2923.
12. Koren, E.; Berkovitch, N.; Rosenwaks, Y. Measurement of Active Dopant Distribution and Diffusion in Individual Silicon Nanowires. *Nano Lett.* **2010,** *10*, 1163–1167.
13. Doh, Y. J.; Maher, K. N.; Ouyang, L.; Yu, C. L.; Park, H.; Park, J. Electrically Driven Light Emission from Individual CdSe Nanowires. *Nano Lett.* **2008,** *8*, 4552–4556.
14. Lind, E.; Persson, A. I.; Samuelson, L.; Wernersson, L.-E. Improved Subthreshold Slope in an InAs Nanowire Heterostructure Field-Effect Transistor. *Nano Lett.* **2006,** *6*, 1842–1846.
15. Ralls, K. S.; Skocpol, W. J.; Jackel, L. D.; Howard, R. E.; Fetter, L. A.; Epworth, R. W.; Tennant, D. M. Discrete Resistance Switching in Submicrometer Silicon Inversion-Layers—Individual Interface Traps and Low-Frequency (1/f?) Noise. *Phys. Rev. Lett.* **1984,** *52*, 228–231.
16. Henry, C. H.; Lang, D. V. Nonradiative Capture and Recombination by Multiphonon Emission in GaAs and GaP. *Phys. Rev. B* **1977,** *15*, 989–1016.
17. Sakr, M. R.; Gao, X. P. A. Temperature Dependence of the Low Frequency Noise in Indium Arsenide Nanowire Transistors. *Appl. Phys. Lett.* **2008,** *93*, 203503.
18. Palma, A.; Godoy, A.; Jimenez-Tejada, J. A.; Carceller, J. E.; Lopez-Villanueva, J. A. Quantum Two-Dimensional Calculation of Time Constants of Random Telegraph Signals in Metal-Oxide-Semiconductor Structures. *Phys. Rev. B* **1997,** *56*, 9565–9574.
19. Lu, M. P.; Chen, M. J. Oxide-Trap-Enhanced Coulomb Energy in a Metal-Oxide-Semiconductor System. *Phys. Rev. B* **2005,** *72*, 235417.
20. Stoneham, A. D. *Theory of Defects in Solids: Electronic Structure of Defects in Insulators and Semiconductors*; Oxford University Press: Oxford, 1975.
21. Pathria, R. K. *Statistical Mechanics*; Pergamon Press: New York, 1972.
22. Kirton, M. J.; Uren, M. J. Noise in Solid-State Microstructures—A New Perspective on Individual Defects, Interface States, and Low Frequency (1/f) Noise. *Adv. Phys.* **1989,** *38*, 367–468.
23. Luryi, S. Quantum Capacitance Devices. *Appl. Phys. Lett.* **1988,** *52*, 501–503.
24. Lee, J.; Spector, H. N. Dielectric Response Function For a Quasi-One-Dimensional Semiconducting System. *J. Appl. Phys.* **1985,** *57*, 366.
25. Mönch, W. *Semiconductor Surfaces and Interfaces*, 3rd ed.; Springer-Verlag: Berlin, 2001; pp 59−65.
26. Hasegawa, H.; He, L.; Ohno, H.; Sawada, T.; Haga, T.; Abe, Y.; Takahashi, H. *Electronic and Microstructural Properties of Disorder-Induced Gap States At Compound Semiconductor-Insulator Interfaces* **1987,** *5*, 1097–1107.
27. McWhorter, P. J.; Winokur, P. S. Simple Technique for Separating the Effects of Interface Traps and Trapped-Oxide Charge in Metal-Oxide-Semiconductor Transistors. *Appl. Phys. Lett.* **1986,** *133*, 135.
28. Liu, F.; Wang, K. L. Correlated Random Telegraph Signal and Low-Frequency Noise in Carbon Nanotube Transistors. *Nano Lett.* **2008,** *8*, 147–151.
29. Ridley, B. K. *Quantum Processes in Semiconductors*, 3rd ed.; Clarendon: Oxford, 1993; pp 252−256.
30. Schwartz, G. P.; Grif_ths, J. E.; Gualtieri, G. J. Thermal-Oxidation and Native Oxide Substrate Reactions on InAs and InxGa1-XAs. *Thin Solid Films* **1982,** *94*, 213–222.

31. Jiang, X.; Xiong, Q.; Nam, S.; Qian, F.; Li, Y.; Lieber, C. M. InAs/InP Radial Nanowire Heterostructures as High Electron Mobility Devices. *Nano Lett.* **2007,** *7*, 3214–3218.
32. Hang, Q.; Wang, F.; Carpenter, P. D.; Zemlyanov, D.; Zakharov, D.; Stach, E. A.; Buhro, W. E.; Janes, D. B. Role of Molecular Surface Passivation in Electrical Transport Properties of InAs Nanowires. *Nano Lett.* **2008,** *8*, 49–55.
33. van Tilburg, J. W. W.; Algra, R. E.; Immink, W. G. G.; Verheijen, M.; Bakkers, E. P. A. M.; Kouwenhoven, L. P. Surface Passivated InAs/InP Core/Shell Nanowires. *Semicond. Sci. Technol.* **2010,** *25*, 024011.
34. Salfi, J.; Savelyev, I. G.; Blumin, M.; Nair, S. V.; Ruda, H. E. Direct Observation of Single-Charge-Detection Capability of Nanowire Field Effect Transistors. *Nat. Nanotechnol.* **2010,** *5*, 737–741.
35. Mueller, H. H.; Worle, D.; Schulz, M. Evaluation of the Coulomb Energy For Single-Electron Interface Trapping in Sub-Micron Metal-Oxide-Semiconductor Field-Effect-Transistors. *J. Appl. Phys.* **1994,** *75*, 2970–2979.
36. Wu, Z. H.; Mei, X. Y.; Kim, D.; Blumin, M.; Ruda, H. E. Growth of Au-Catalyzed Ordered GaAs Nanowire Arrays by Molecular-Beam Epitaxy. *Appl. Phys. Lett.* **2002,** *81*, 5177–5179.
37. Wunnicke, O. Gate Capacitance of Back-Gated Nanowire Field-Effect Transistors. *Appl. Phys. Lett.* **2006,** *89*, 083102.
38. Giusi, G.; Crupi, F.; Pace, C. An Algorithm for Separating Multilevel Random Telegraph Signal from 1/*f* Noise. *Rev. Sci. Instrum.* **2008,** *79*, 024701.
39. House, M. G.; Jiang, H. W.; Zhang, X. C. Analysis of Electron Tunneling Events with the Hidden Markov Model. *Phys. Rev. B* **2009,** *80*, 113308.